



Practitioner's Docket No. 6353/P1/DSM/LOW K/JW

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Howard Li, et al.

Application No.: 10/759,801

Group No.: 1753

Filed: January 16, 2004

Examiner: N/A

For: INTEGRATED EQUIPMENT SET FOR FORMING A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE

Mail Stop Petition

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

PETITION TO ACCORD CORRESPONDENCE FILING DATE SHOWN
ON EXPRESS MAIL LABEL "DATE-IN"
(37 C.F.R. 1.10(c))

1. This is a petition to accord the correspondence in the above-identified Application the "date-in" of January 16, 2004 shown on the Express Mail Label No. EL975550261US.

It is respectfully contended that the date of January 20, 2004 accorded this correspondence by the PTO is incorrect.

2. Submitted herewith is the statement of Robert W. Mulcahy as to when the discrepancy was discovered relating to this petition being filed promptly thereafter. 37 C.F.R. 1.10(c)(1).

3. Attached is a true copy of the first page of the correspondence which was filed, showing that the number of the Express Mail label was placed thereon prior to mailing. 37 C.F.R. 1.10(c)(2).

4. Attached is true copy of the "Express Mail" mailing label showing the "date-in" of January 16, 2004. 37 C.F.R. 1.10(c)(3). *Note that our return receipt postcard (copy attached) shows a filing date of January 16, 2004 for this application (U.S. Patent Application Serial No. 10/759,801).*

CERTIFICATE OF MAILING/TRANSMISSION (37 C.F.R. Section 1.8(a))

I hereby certify that, on the date shown below, this correspondence is being:

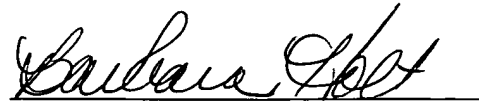
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☒ deposited with the United States Postal Service with sufficient postage as Express Mail in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450

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☐ transmitted by facsimile to the Patent and Trademark Office (703) ____-____.


Signature

BARBARA HOLT
(type or print name of person certifying)

Date:

June 17, 2004

5. Other attachments: A copy of the Patent Application Cover Sheet containing Express Mail Certificate.

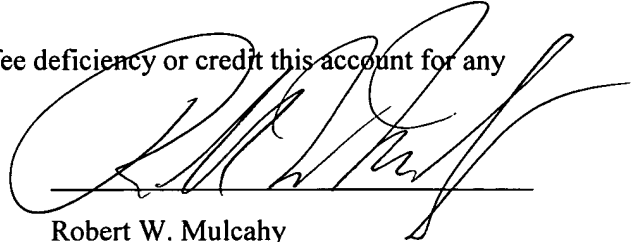
6. The petition fee is paid as follows:

Please charge the petition fee to deposit account no. 50-1074.

A duplicate of this petition is enclosed.

Please charge Account No. 50-1074 for any fee deficiency or credit this account for any overpayment for this petition.

Date:

A handwritten signature in black ink, appearing to read 'R. W. Mulcahy', is written over a horizontal line.

Robert W. Mulcahy
Registration No. 25,436

MAIL STOP PATENT APPLICATION

Commissioner for Patents

P.O. Box 1450

Alexandria, VA 22313-1450

Applicant(s): Howard Li et al.

Assignee: Applied Materials, Inc.Title: INTEGRATED EQUIPMENT SET FOR FORMING A LOW K
DIELECTRIC INTERCONNECT ON A SUBSTRATE

Serial No.: unknown Filed: herewith

Docket No.: 6353/P1/LOW K/JW

Enclosed:

- ☒ Patent Application Transmittal
- ☒ Specification, claims and abstract - 124 pgs.
- ☒ Drawings (forty-three pages) Informal
- ☒ Return Receipt postcards

Dated: January 16, 2004

Express Mail Label No. EL975550261US

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15535 U.S. PTO
10/759801

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APPLICATION FOR UNITED STATES LETTERS PATENT

APPLICANT(S): HOWARD LI
LEE LUO
ILIAS ILIOPOULOS
MICHAEL ARMACOST


TITLE: INTEGRATED EQUIPMENT SET FOR
FORMING A LOW K DIELECTRIC
INTERCONNECT ON A SUBSTRATE

DOCKET NO.: 6353/P1/LOW K/JW

APPLIED MATERIALS, INC.

CERTIFICATE OF MAILING UNDER 37 CFR 1.10

I hereby certify that, on the date shown below, this correspondence is being deposited with the United States Postal Service in an envelope addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, as "Express Mail Post Office to Addressee" Mailing Label No.: EL975550261US on January 16, 2004.

Name of person mailing papers: Brian M. Dugan
 1/16/04
Signature Date

DUGAN & DUGAN, P.C.
18 John Street
Tarrytown, New York 10591
(914)332-9081



PATENTS
6353/P1/DSM/LOW K/JW

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s) : Howard Li, et al.
Serial No. : 10/759,801
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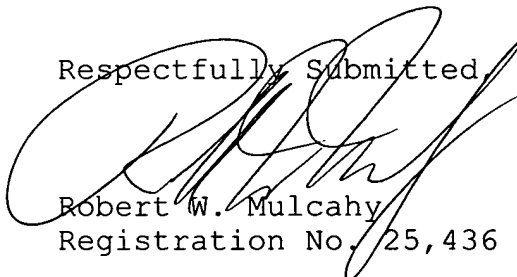
Mail Stop Petition
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

STATEMENT OF PROMPTNESS OF FILING
OF PETITION TO CORRECT FILING DATE

Sir:

In accordance with 37 C.F.R. § 1.10 (d)(1), I, Robert W. Mulcahy, state that the discrepancy in the filing date for the above-identified patent application was not discovered until after we received a copy of the Notice to File Missing Parts for this case on or about April 29, 2004. Accordingly, the enclosed Petition is being filed promptly.

Respectfully Submitted,



Robert W. Mulcahy
Registration No. 25,436

Dated:

INTEGRATED EQUIPMENT SET FOR FORMING
A LOW K DIELECTRIC INTERCONNECT ON A SUBSTRATE

This application claims priority from U.S.

- 5 Provisional Patent Application Serial No. 60/440,898, filed
January 16, 2003 and is a continuation-in-part of U.S.
Patent Application Serial No. 10/459,194, filed June 11,
2003, which claims priority from U.S. Provisional Patent
Application Serial No. 60/387,835, filed June 11, 2002. All
10 of the above listed patent applications are hereby
incorporated by reference herein in their entirety.

CROSS REFERENCE TO RELATED APPLICATIONS

- This application is related to U.S. Provisional
15 Patent Application Serial No. 60/323,065, filed September
18, 2001 and titled "INTEGRATED EQUIPMENT SET FOR FORMING AN
INTERCONNECT ON A SUBSTRATE", which is hereby incorporated
by reference herein in its entirety.

This application also is related to U.S.

- 20 Provisional Patent Application Serial No. 60/333,901, filed
November 28, 2001 and titled "INTEGRATED EQUIPMENT SET FOR
FORMING SHALLOW TRENCH ISOLATION REGIONS", which is hereby
incorporated by reference herein in its entirety.

25 FIELD OF THE INVENTION

The present invention relates to semiconductor
device manufacturing, and more specifically to an integrated
equipment set for forming a low K dielectric interconnect on
a substrate.

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BACKGROUND OF THE INVENTION

- A typical integrated circuit contains a plurality
of metal pathways that provide electrical power for powering
the various semiconductor devices forming the integrated
35 circuit, and that allow these semiconductor devices to